

LOW POWER MOBILE SoC

**ON-CHIP CLOCK DISTRIBUTION** 

INTERNET OF THINGS

**AUTOMOTIVE** 

DDR/LPDDR PCle

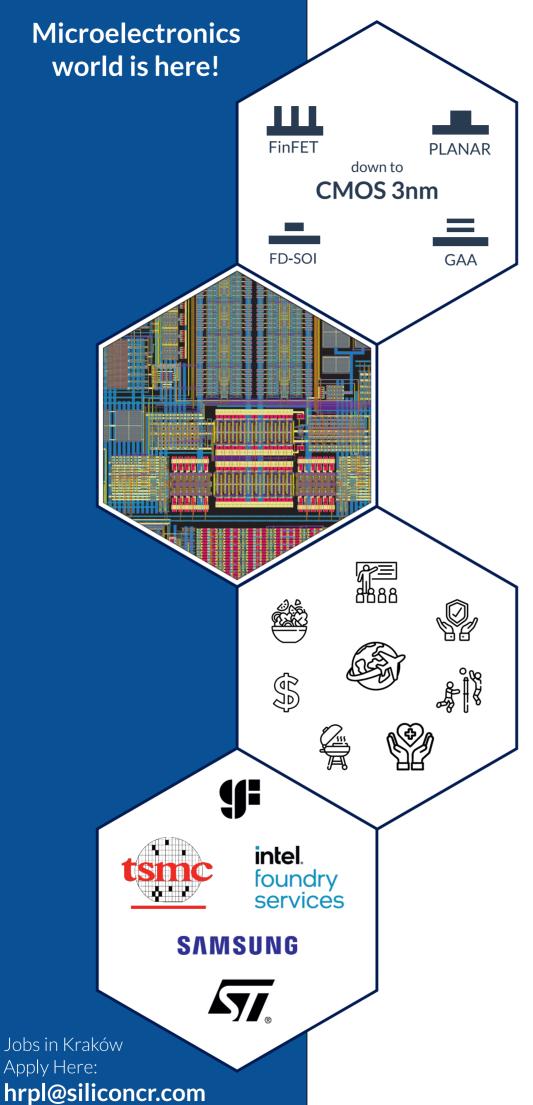
LC-PLL & RING-PLL up to 18GHz

MULTI-PROTOCOL SERDES

32Gbps and more

Majority of World's **TOP 50 INTEGRATED CIRCUITS** companies work with us!





## Hardware Verification & Validation Engineer

- multidisciplinary, hardwareengineering tasks
- · high-speed digital design
- high-end measurement equipment
- PCB & Systems design
  (Altium Designer / Keysight ADS)
- Signal Integrity, Power Integrity
- debugging, testing and reporting
- MATLAB/Python/Git/SCPI/FPGA

#### Analog & Mixed-Signal Layout Design Engineer

- developing layout of integrated circuits
- post-layout simulation & verification
- product-related documentation
- product development & maintenance
- customer support
- Silvaco Expert/Cadence Virtuoso

#### **Mixed-Signal Design Engineer**

- simulation of the mixed-signal circuits
- test plans and testbenches
- analysis & visualization of simulation results
- SPICE, scripting, Python
- Silvaco Gateway

#### **Digital Design/Verification Engineer**

- generation & verification of Verilog behavioral models
- design & verification of RTL blocks
- scripting infrastructure & verification metholodogies
- supporting industry-leading customers
- Verilog/SystemVerilog
- Perl/Python/Bash

#### **IP Library Characterization Engineer**

- development of timing model libraries of PLL/SerDes/LVDS products
- development of internal characterization flow
- design of verification methodologies
- customer support
- analysis & visualization
- SPICE
- Python/Perl/Bash/TCL

### **Physical Design Engineer**

- Full chip integration
- Synthesis, Floorplanning, Place&Route, Tape-out
- Timing analyses
- PerI/Python/Bash/TCL

# Automotive Functional Safety Engineer

- ISO26262
- reliability analysis
- FMEDA, FTA, FIT
- safety manual & documentation
- Perl/Matlab/Verilog/Python